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Document Title **LAT Tracker Front-end Readout Chip Wafer Test Procedure**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Tracker Front-end Readout Chip Wafer Test Procedure

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
v1.0	August 29, 2001	First version
v2.0	October 14, 2001	Scope, test condition, and chip rating sections are added
v3.0	November 9, 2001	Reformatted; more tests added
v4.0	June 20, 2002	Test procedure polished

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1 Purpose

This report serves to document the test plan of the GLAST LAT Tracker front-end (GTFE) ASIC wafers. These tests are carried out on all ASIC's on all wafers for initial prototype assemblies and for TMCM assemblies for GLAST LAT Tracker production.

2 Scope

The GLAST LAT Tracker will be instrumented with about 80 m^2 of silicon strip detectors (SSD) and nearly 900,000 channels of electronics. The SSD's are assembled onto the two sides of composite "tray" panels, of which 19 are stacked into each of the 18 towers. Each layer of SSD's is read out by an electronics module (TMCM), mounted on the edge of the tray panel. Extensive testing of the electronics is done during assembly at the component level (ASIC and TMCM) and at the tray level. The hardware systems for those tests are described in [11]. The procedures for wafer testing of the ASIC's to be mounted on TMCM's are documented in this document and [15]. The procedures for the electrical testing of the TMCM's after all components have been mounted and wire bonding within the TMCM is complete is documented in [16]. This plan covers the electrical testing of the tracker front-end readout ASIC wafers before the wafers are diced into chips. The environmental and electrical test plans of the completed towers are specified in [13] and [17].

3 Definitions

3.1 Acronyms

ASIC — Application Specific Integrated Circuit
DAC — Digital-to-Analog Converter
FIFO — First-in, First-out
GLAST — Gamma-ray Large Area Space Telescope
GTFE — GLAST Tracker Front-end Electronics
LAT — Large Area Telescope
MIP — Minimum Ionizing Particle
PWB — Printed Wiring Board
SSD — Silicon Strip Detector
TEM — Tracker Electronics Module
TMCM — Tracker Multi-Chip Module

3.2 Names of Signal lines

Signal name	Meaning
TRIG_LI	LVDS pair of TRIG_LIP and TRIG_LIM
TRIG_LO	LVDS pair of TRIG_LOP and TRIG_LOM
TRIG_RI	LVDS pair of TRIG_RIP and TRIG_RIM
TRIG_RO	LVDS pair of TRIG_ROP and TRIG_ROM
DATA_LI	LVDS pair of DATA_LIP and DATA_LIM
DATA_LO	LVDS pair of DATA_LOP and DATA_LOM
DATA_RI	LVDS pair of DATA_RIP and DATA_RIM
DATA_RO	LVDS pair of DATA_ROP and DATA_ROM
CMDL	LVDS pair of CMDLP and CMDLM
CMDR	LVDS pair of CMDRP and CMDRM
CLKL	LVDS pair of CLKLP and CLKLM
CLKR	LVDS pair of CLKRP and CLKRM
TACKL	LVDS pair of TACKLP and TACKLM
TACKR	LVDS pair of TACKRP and TACKRM

3.3 Names of GTFE Commands

Command name	Function code	Meaning of the command
NOP	00000	No operation
RST_CHIP	00010	Reset chip
CALIBRATE	00011	Generate a calibration strobe
READ_EVENT	00100	Start the event read-out sequence
LD_CHN_MSK	01000	Load GTFE Channel Mask
LD_CAL_MSK	01001	Load GTFE Calibration Mask
LD_TRG_MSK	01010	Load GTFE Trigger Mask
LD_TH/C_DAC	01011	Load GTFE Threshold and Calibration DAC's
LD_MUTE	01100	Load GTFE MODE register
RD_CHN_MSK	10000	Read GTFE Channel Mask
RD_CAL_MSK	10001	Read GTFE Calibration Mask
RD_TRG_MSK	10010	Read GTFE Trigger Mask
RD_TH/C_DAC	10011	Read GTFE Threshold and Calibration DAC's
RD_MUTE	10100	Read GTFE MODE register

4 References

[1] LAT-TD-00156 LAT Tracker Preliminary Design Report
[2] LAT-SS-00017 LAT TKR Subsystem Specification — Level III Specification
[3] LAT-SS-00134 LAT TKR Subsystem Specification — Level IV Specification
[4] LAT-SS-00152 LAT TKR Subsystem Specification — Level IV Readout Electronics Requirements
[5] LAT-SS-00168 Conceptual Design of the LAT Tracker Electronics Readout System
[6] LAT-SS-00169 Tracker Front- End Readout ASIC Specification
[7] LAT-SS-00170 Conceptual Design of the GLAST Tracker Readout Controller Electronics ASIC (GTRC)
[8] LAT-SS-00171 Specification of the LAT Tracker front-end readout Multi-Chip Module (TMCM)
[11] LAT-TD-00153 Test Systems for the GLAST Tracker Front-End Electronics
[12] LAT-SS-00176 Tracker Electrical Interface Specification
[13] LAT-TD-00154 LAT Tracker Tray Test Plan
[14] LAT-TD-00155 LAT Tracker Tower Test Plan
[15] LAT-TD-00248 LAT Tracker Readout Controller Chip Wafer Test Procedure
[16] LAT-TD-00249 GLAST LAT Tracker TMCM Test Procedures
[17] LAT-TD-00191 LAT Tracker Tower Electrical Test Plan

5 Tracker Tower Description

The conceptual design of the Tracker tower modules is described in the Preliminary Design Report[1]. The conceptual design of the read-out electronics is described in [5], and detailed specifications for the components of the design are found in [6], [7], [8], [9], and [10]. The electrical interface of the Tracker read-out to the TEM is described in [12].

The requirements for the Tracker electronics read-out are specified in [2], [3], and [4]. The tests described here refer to those documented requirements.

6 Test System

All of the tests described herein require the following ground support equipment: a probe card, an interface PWB with LVDS drivers/receivers, a VME I/O module, a VME-based ADC module, a VME Crate, a VME crate controller, a PC with a VEM interface card and a GPIB interface card, and power suppiles. The hardware configuration of the equipment is described in [11].

All GTFE wafers are tested under a special condition/environment other than the normal operation condition/environment for GTFE chips in order to ensure effective screening of problematic chips with conservative safety margins. The test condition in the following table should be applied unless otherwise specified in the test procedures.

	Test condition	Normal operation
Clock frequency	25 MHz	20 MHz
Analog power supply voltage (AVDDA)	1.3 V	1.5 V
Analog power supply voltage (AVDDB)	2.2 V	2.5 V
Digital power supply voltage (DVDD)	2.2 V	2.5 V
Temperature	60 °C	—

7 Test Procedures

All the test procedures for GTFE chips in the GLAST LAT tracker construction is described below. Some of the tests should be performed only once through the left command decoder, and the others should be repeated twice, once through the left command decoder and another time through the right command decoder. The former is designated by "LEFT only" in the test description, and the latter "LEFT and RIGHT".

7.1 Common Settings and Procedures

There are the settings and the procedures that should be applied to all the test procedures described in this section. Follow the instructions listed below in all the tests unless otherwise specified.

- Use a signal line in parentheses for the test through the right command decoder.
- Set 21 (10101 in binary) to a chip address (GTFE pins A0 – A4) and to an address in a command, unless otherwise specified.
- Use write address 2 (two) for a trigger signal placed on TACKL and TACKR, unless otherwise specified.
- Use read address 2 (two) for a READ_EVENT command, unless otherwise specified.
- Supply a clock to both command decoder at all times.

The following calibration constants for Threshold and Calibration DAC's are assumed for the tests listed below. Relevant parameters for the DAC settings in each test are indicated in parentheses following the DAC value and range in the test procedure below. If the calibration constants are revised or changed in the future, the settings of Threshold and Calibration DAC's should be changed throughout the test procedure accordingly.

- The following formula for Threshold DAC:

$$\begin{aligned} V &= 4.5 + 4.5 \times n \quad \text{for low range} \\ V &= 12.9 + 12.9 \times n \quad \text{for high range} \end{aligned}$$

  where V is the DAC output voltage in mV, n is the DAC value
- The following formula for Calibration DAC:

$$\begin{aligned} V &= 1.57 + 1.53 \times n \quad \text{for low range} \\ V &= 15.0 + 14.6 \times n \quad \text{for high range} \end{aligned}$$

  where V is the DAC output voltage in mV, n is the DAC value
- 46 fF for coupling capacitance on the test input for charge injections
- 100 mV/fC for the nominal shaper gain

7.2 Power Consumption Tests

7.2.1 Power Consumption

Test	TF101	**Direction**	N/A
Prerequisite	None		
Purpose	Measure the GTFE power consumption.		
Method	Measure the current draws into the power lines (DVDD, AVDDA, and AVDDB) and the current biases (IBIAS and IFET).		
Specification	?? $< I_{\mathrm{DVDD}} <$??, ?? $< I_{\mathrm{AVDDA}} <$??, ?? $< I_{\mathrm{AVDDB}} <$??, ?? $< I_{\mathrm{IBIAS}} <$??, and ?? $< I_{\mathrm{IFET}} <$??. (The acceptance ranges are to be determined.)		

1. Supply 2.5 V on DVDD (digital power), 1.5 V on AVDDA (analog power), and 2.5 V on AVDDB (analog power).
2. Supply a 20 MHz clock to both command decoders.
3. Measure the current draw into DVDD, AVDDA, AVDDB, IBIAS (current bias for analog circuitry), and IFET (current bias for input transistor).
4. Record the current draws.
5. Confirm that the resulting current draws are within specifications.

7.3 Functionality Tests

7.3.1 Configuration register load and read-back

Test	TF201	**Direction**	LEFT & RIGHT
Prerequisite	Power test, TF101.		
Purpose	Test loading and reading back the configuration registers.		
Method	Load and read back the configuration registers.		
Specification	Register contents read back must be identical to those loaded. All the bits in the register must be able to be set to 0 (zero) and to 1 (one). Read-back response must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT (RIGHT) decoder.
2. Send a LD_CHN_MSK command to mask all but channels 0, 3, 6, ..., and 63.
3. Send a RD_CHN_MSK command and record a bit stream on CTRLREG.
4. Compare the bit stream with the intended contents.
5. Repeat steps 2–4 with masking all but channels 1, 4, 7, ..., and 61.
6. Repeat steps 2–4 with masking all but channels 2, 5, 8, ..., and 62.
7. Repeat steps 2–6 with LD_CAL_MSK commands.
8. Repeat steps 2–6 with LD_TRG_MSK commands.
9. Send a LD_TH/C_DAC command to set:
   - 21 (010101 in binary), high range to Threshold DAC,
   - 42 (101010 in binary), low range to Calibration DAC.
10. Send a RD_TH/C_DAC command and record a bit stream on CTRLREG.
11. Compare the bit stream with the intended contents.
12. Repeat steps 9–11 with setting:
    - 42 (101010 in binary), low range to Threshold DAC,
    - 21 (010101 in binary), high range to Calibration DAC.
13. Send a LD_MUTE command to select the LEFT decoder and set a DEAF bit.
14. Send a RD_MUTE command and record a bit stream on CTRLREG.
15. Compare the bit stream with the intended contents.
16. Repeat steps 13–15 with selecting the RIGHT decoder and unsetting a DEAF bit.

7.3.2 Calibration mask test

Test	TF202	**Direction**	LEFT only
Prerequisite	Configuration register load and read-back, TF201.		
Purpose	Test injecting charges to selected channels.		
Method	Inject charges to selected channels to fire the comparators, record the event, and read it out. A layer-OR signal must appear in response to the charge injection, and a hit must be recorded on the selected channels.		
Specification	All channels must respond to the charge injection. It must be possible to disable any subset of channels from the charge injection. Data read out must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL. Then, record a logic state of TRIG_LO.
4. Confirm that TRIG_LO state changes in response to the charge injection.
5. Send a READ_EVENT command. Then, record a bit stream on DATA_LO.
6. Confirm that a hit appears on channels 0, 3, 6, ..., and 63 only.
7. Repeat steps 2–5 with setting Calibration Mask to mask all but channels 1, 4, 7, ..., and 61.
8. Confirm that a hit appears on channels 1, 4, 7, ..., and 61 only.
9. Repeat steps 2–5 with setting Calibration Mask to mask all but channels 2, 5, 8, ..., and 62.
10. Confirm that a hit appears on channels 2, 5, 8, ..., and 62 only.

7.3.3 Channel mask test

Test	TF203	**Direction**	LEFT only
Prerequisite	Calibration mask test, TF202.		
Purpose	Test that all channels can be masked from the data.		
Method	Injects charges to selected channels to fire the comparators with Channel Mask masking the selected channels, record the event, and read it out. No hit must appear in the recorded event with layer-OR response detected.		
Specification	It must be possible to disable any subset of channels from the data stream. Data read out must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT decoder.
2. Set the Configuration Register as follows:

Channel Mask	mask channels 0, 3, 6, ..., and 63
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL. Then, record a logic state of TRIG_LO.
4. Confirm that TRIG_LO state changes in response to the charge injection.
5. Send a READ_EVENT command. Then, record a bit stream on DATA_LO.
6. Confirm that a hit does not appear on any channel.
7. Repeat steps 2–5 with setting Channel Mask to mask channels 1, 4, 7, ..., and 61 and Calibration Mask to mask all but channels 1, 4, 7, ..., and 61.
8. Confirm that a hit does not appear on any channel.
9. Repeat steps 2–5 with setting Channel Mask to mask channels 2, 5, 8, ..., and 62 and Calibration Mask to mask all but channels 2, 5, 8, ..., and 62.
10. Confirm that a hit does not appear on any channel.

7.3.4 Trigger mask test

Test	TF204	**Direction**	LEFT only
Prerequisite	Channel mask test, TF203.		
Purpose	Test that all channels can be masked from the trigger.		
Method	Inject charges to selected channels to fire the comparators with Trigger Mask masking the selected channels, record the event, and read it out. A layer-OR signal must not appear in response to the charge injection, and a hit must be recorded on the selected channels.		
Specification	It must be possible to disable any subset of channels from the layer-OR. Data read out must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	mask channels 0, 3, 6, ..., and 63
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL. Then, record a logic state of TRIG_LO.
4. Confirm that TRIG_LO state changes in response to the charge injection.
5. Send a READ_EVENT command. Then, record a bit stream on DATA_LO.
6. Confirm that a hit appears on channels 0, 3, 6, ..., and 63 only.
7. Repeat steps 2–5 with setting Trigger Mask to mask channels 1, 4, 7, ..., and 61 and Calibration Mask to mask all but channels 1, 4, 7, ..., and 61.
8. Confirm that a hit appears on channels 1, 4, 7, ..., and 61 only.
9. Repeat steps 2–5 with setting Trigger Mask to mask channels 2, 5, 8, ..., and 62 and Calibration Mask to mask all but channels 2, 5, 8, ..., and 62.
10. Confirm that a hit appears on channels 2, 5, 8, ..., and 62 only.

7.3.5 Calibration and Threshold DAC's test

Test	TF205	**Direction**	LEFT only
Prerequisite	Calibration mask test, TF202.		
Purpose	Test the Calibration and Threshold DAC outputs.		
Method	Inject the various amount of charges to selected channels with various levels of threshold set, record the event, and read it out. The layer-OR response and the hit information in the data must be as expected from the relationship between the amount of charge and the threshold voltage.		
Specification	It must be possible to change the Threshold and Calibration DAC's output voltages. Data read out must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL. Then, record a logic state of TRIG_LO.

4. Confirm that TRIG_LO state changes in response to the charge injection.
5. Send a READ_EVENT command. Then, record a bit stream on DATA_LO.
6. Confirm that a hit appears on channels 0, 3, 6, ..., and 63 only.
7. Repeat steps 2–5 with setting Calibration DAC to 27, low range ($\approx$ 200 mV at the shaper output).
8. Confirm that a logic state of TRIG_LO does not change in response to the charge injection, and that a hit does not appear on any channel.
9. Repeat steps 2–5 with setting Threshold DAC to 11, high range ($\approx$ 150 mV) and Calibration DAC to 7, high range ($\approx$ 550 mV at the shaper output).
10. Confirm that a logic state of TRIG_LO changes in response to the charge injection, and that a hit appears on channels 0, 3, 6, ..., and 63 only.

7.3.6 Hard and soft reset

Test	TF206	**Direction**	LEFT & RIGHT
Prerequisite	Calibration mask test, TF202.		
Purpose	Test the hard and soft reset functions.		
Method	Inject charges to selected channels to fire the comparators, record the event, read it out, and reset the chip while the data is being read out. Also, read out the configuration register contents after the reset. The reset is initiated by a reset command and a reset pulse.		
Specification	The chip must stops sending out the data immediately when the reset becomes in effect. The register contents read back must match the power-on default specification. Data read out must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT (RIGHT) decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT (RIGHT) decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL (TACKR).
4. Send a READ_EVENT command, then a RST_CHIP command after 30 clock cycles. Record a bit stream on DATA_LO (DATA_RO).
5. Confirm that a hit appears on channels 0, 3, 6, ..., and 63 until the RST_CHIP command is in effect.
6. Send a RD_CHN_MSK command, a RD_CAL_MSK command, a RD_TRG_MSK command, a RD_TH/C_DAC command, and a RD_MUTE command, and record a bit stream on CTRLREG.
7. Confirm that the register contents are reset to the power-on default.
8. Repeat steps 2–4 with sending a pulse on RESET instead of a RST_CHIP command.
9. Confirm a hit appears on channels 0, 3, 6, ..., and 63 until the RESET pulse is in effect.
10. Repeat steps 6–7.

7.3.7 FIFO memory test

Test	TF207	**Direction**	LEFT only
Prerequisite	Calibration mask test, TF202.		
Purpose	Test all bits in the FIFO memory.		
Method	Inject charges to selected channels to fire the comparators, record the event to set 1 (one) to the selected bits in the FIFO memory, and read it out. The selected bits must be set to 1 (one) and the others to 0 (zero).		
Specification	All bits in any depths of the FIFO memory must be able to set to 0 (zero) and to 1. Data read out must be in correct data format.		

1. Send a LD_MUTE register command to select the LEFT decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 4, 8, ..., and 60
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL with write address 0 (zero).
4. Repeat steps 2–3 for each of the following settings:
   (a) write address 1 and Calibration Mask to mask all but channels 1, 5, 9, ..., and 61
   (b) write address 2 and Calibration Mask to mask all but channels 2, 6, 10, ..., and 62
   (c) write address 3 and Calibration Mask to mask all but channels 3, 7, 11, ..., and 63
5. Send a READ_EVENT command with read address 0 (zero). Record a bit stream on DATA_LO (DATA_RO).
6. Confirm that a hit appears every fourth channel starting from channel 0 (zero).
7. Repeat step 5 with read address 1, 2, and 3.
8. Confirm that a hit appears every fourth channel starting from channel 1, 2, and 3 accordingly.
9. Repeat steps 2–3 for each of the following settings:
   (a) write address 0 and Calibration Mask to mask all but channels 1, 5, 9, ..., and 61
   (b) write address 1 and Calibration Mask to mask all but channels 2, 6, 10, ..., and 62
   (c) write address 2 and Calibration Mask to mask all but channels 3, 7, 11, ..., and 63
   (d) write address 3 and Calibration Mask to mask all but channels 0, 4, 8, ..., and 60
10. Repeat step 5 with read address 0, 1, 2, and 3.
11. Repeat steps 2–3 four times, once each for each of the following settings:
    (a) write address 0 and Calibration Mask to mask all but channels 2, 6, 10, ..., and 62
    (b) write address 1 and Calibration Mask to mask all but channels 3, 7, 11, ..., and 63
    (c) write address 2 and Calibration Mask to mask all but channels 0, 4, 8, ..., and 60
    (d) write address 3 and Calibration Mask to mask all but channels 1, 5, 9, ..., and 61
12. Repeat step 5 with read address 0, 1, 2, and 3.
13. Repeat steps 2–3 four times, once each for each of the following settings:
    (a) write address 0 and Calibration Mask to mask all but channels 3, 7, 11, ..., and 63
    (b) write address 1 and Calibration Mask to mask all but channels 0, 4, 8, ..., and 60
    (c) write address 2 and Calibration Mask to mask all but channels 1, 5, 9, ..., and 61
    (d) write address 3 and Calibration Mask to mask all but channels 2, 6, 10, ..., and 62
14. Repeat step 5 with read address 0, 1, 2, and 3.

7.3.8 Chip-to-chip transfer of layer-OR signals

Test	TF208	**Direction**	LEFT & RIGHT
Prerequisite	Channel and Trigger mask tests, TF203 and TF204.		
Purpose	Test transferring layer-OR signals between chips.		
Method	Place certain pulses on the layer-OR input and monitor the output, once with DEAF mode OFF and the other time with DEAF mode ON.		
Specification	The input pulses must be repeated on the output with DEAF mode OFF. They must not with DEAF mode ON.		

1. Send a LD_MUTE command to select the LEFT (RIGHT) decoder.
2. Set the Configuration Register as follows:

Channel Mask	mask all channels
Calibration Mask	mask all channels
Trigger Mask	mask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT (RIGHT) decoder, unset a DEAF bit

3. Place a bit stream on TRIG_LI (TRIG_RI) and record a bit stream on TRIG_LO (TRIG_RO).
4. Confirm that TRIG_LO (TRIG_RO) changes in response to the bit stream on TRIG_LI (TRIG_RI).
5. Repeat steps 2–3 with setting a DEAF bit in the GTFE MODE register.
6. Confirm that TRIG_LO (TRIG_RO) does not change in response to the bit stream on TRIG_LI (TRIG_RI).
7. Repeat steps 2–3 with setting 0 (23 for RIGHT) to a chip address.
8. Confirm that TRIG_LO (TRIG_RO) changes in response to the bit stream on TRIG_LI (TRIG_RI).
9. Repeat steps 2–3 with setting 23 (0 for RIGHT) to a chip address.
10. Confirm that TRIG_LO (TRIG_RO) does not change in response to the bit stream on TRIG_LI (TRIG_RI).

7.3.9 Chip-to-chip transfer of data signals

Test	TF209	**Direction**	LEFT & RIGHT
Prerequisite	Channel mask test, TF203.		
Purpose	Test transferring data signals between chips.		
Method	Inject charges to selected channels to fire the comparators, record the event, and read it out with a certain bit pattern placed on the data input, once with DEAF mode OFF and the other time with DEAF mode ON. Also, the test is performed with no hit generated.		
Specification	The bit pattern on the input must be repeated on the output with DEAF mode OFF. It must not with DEAF mode ON. Zero-suppression in the data stream must be in effect in the case of no hit.		

1. Send a LD_MUTE command to select the LEFT (RIGHT) decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT (RIGHT) decoder, unset a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL (TACKR).
4. Send a READ_EVENT command and place some bit stream on DATA_LI (DATA_RI) at the same time. Record a bit stream on DATA_LO (DATA_RO).
5. Confirm that a hit appears on channels 0, 3, 6, ..., and 63, followed by the bit stream placed on DATA_LO (DATA_RO).
6. Repeat steps 2–4 with setting a DEAF bit in the GTFE MODE register.
7. Confirm that a hit appears on channels 0, 3, 6, ..., and 63, and that the bit stream placed on DATA_LO (DATA_RO) does not follow.
8. Repeat steps 2–4 with setting Channel Mask to mask all channels.
9. Confirm that a hit does not appear on any channel, and that the bit stream placed on DATA_LO (DATA_RO) follows immediately after the HIT bit in data output.
10. Repeat steps 2–4 with setting 0 (23 for RIGHT) to a chip address.

11. Confirm that a hit appears on channels 0, 3, 6, ..., and 63, and that the bit stream placed on DATA_LO (DATA_RO) does not follow.
12. Repeat steps 2–4 with setting 23 (0 for RIGHT) to a chip address.
13. Confirm that a hit does not appear on any channel, and that the bit stream placed on DATA_LO (DATA_RO) follows immediately after the HIT bit in data output.

7.3.10 Address decoding

Test	TF210	**Direction**	LEFT & RIGHT
Prerequisite	Calibration mask test, TF202.		
Purpose	Test the address decoding function.		
Method	Inject charges to selected channels to fire the comparators, record the event, and read it out with all the possible combinations of a hard-wired address and an address in a read-out command.		
Specification	The event must be able to be read-out only in the cases in which the addresses given match or a read-out command is sent with a broadcast address. Data read out must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT (RIGHT) decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT (RIGHT) decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL (TACKR).
4. Set 0 (zero) to the hard-wired chip address (GTFE pins A0 – A4).
5. Send a READ_EVENT command with address 0, 1, 2, ..., 31 in the command. Record a bit stream on DATA_LO (DATA_RO).
6. Confirm that a hit appears on channels 0, 3, 6, ..., and 63 only when the address in the READ_EVENT command matches to the hard-wired chip address or 31 (broadcast address).
7. Repeat steps 4–6 for the hard-wired address of 1, 2, 3, ..., and 31.

7.3.11 Response to undefined command

Test	TF211	**Direction**	LEFT & RIGHT
Prerequisite	Calibration mask test, TF202.		
Purpose	Test chip response to undefined commands.		
Method	After sending an undefined command or a NOP command, inject charges to selected channels to fire the comparators, record the event, and read it.		
Specification	The event must be able to be read-out correctly. Data read out must be in correct data format.		

1. Send a LD_MUTE command to select the LEFT (RIGHT) decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 3, 6, ..., and 63
Trigger Mask	unmask all channels
Threshold DAC	47, high range ($\approx$ 620 mV)
Calibration DAC	27, high range ($\approx$ 1.9 V at the shaper output)
MODE register	select LEFT (RIGHT) decoder, set a DEAF bit

3. Send a command with function code 00000 and with a dummy 68-bit data.
4. Send a CALIBRATE command and place a trigger signal on TACKL (TACKR).

5. Send a READ_EVENT command. Then, record a bit stream on DATA_LO (DATA_RO).
6. Confirm that a hit appears on channels 0, 3, 6, ..., and 63.
7. Repeat steps 3–6 for function codes 00001, 00101, 00110, 00111, 01101, 01110, 01111, 10101, 10110, 10111, 11000, 11001, 11010, 11011, 11100, 11101, 11110, and 11111.

7.3.12 Amplifier gain estimate

Test	TF301	**Direction**	LEFT only
Prerequisite	Trigger mask test, TF204, Calibration and Threshold DAC's test, TF205, and FIFO memory test, TF207.		
Purpose	Identify channels on which amplifier gain is too low or too high.		
Method	Inject charges of approximately 1 MIP (5.3 fC) to selected channels with threshold at 0.75 MIP and at 1.25 MIP, record the event, and read it out.		
Specification	Gain of all channels must be within 25 % off of the nominal gain. Data read out must be in correct data format.		

1. Send a LD_MUTE register command to select the LEFT decoder.
2. Set the Configuration Register as follows:

Channel Mask	unmask all channels
Calibration Mask	mask all but channels 0, 4, 8, ..., and 60
Trigger Mask	mask all channels
Threshold DAC	30, high range ($\approx$ 400 mV)
Calibration DAC	7, high range ($\approx$ 5.5 fC charge injection)
MODE register	select LEFT decoder, set a DEAF bit

3. Send a CALIBRATE command and place a trigger signal on TACKL with write address 0 (zero).
4. Repeat steps 2–3 for each of the following settings:
   (a) write address 1 and Calibration Mask to mask all but channels 1, 5, 9, ..., and 61
   (b) write address 2 and Calibration Mask to mask all but channels 2, 6, 10, ..., and 62
   (c) write address 3 and Calibration Mask to mask all but channels 3, 7, 11, ..., and 63
5. Send a READ_EVENT command with read address 0 (zero). Record a bit stream on DATA_LO.
6. Confirm that a hit appears every fourth channel starting from channel 0 (zero). If a hit does not appear on some of the channels, the gain of the channels is lower than the nominal gain by 25 % or larger.
7. Repeat step 5 with read address 1, 2, and 3.
8. Send a LD_TH/C_DAC command to set 52, high range ($\approx$ 680 mV) to Threshold DAC.
9. Repeat steps 2–7.
10. Confirm that a hit does not appear on any channel. If a hit appears on some of the channels, the gain of the channels is higher than the nominal gain by 25 % or larger.

8 Chip Rating and Acceptance Criteria

All tested GTFE chips are rated in three ranks based on the test results. Depending on its chip rating, a tested chip is to be assembled onto a TMCM, rejected from the assembly (unused at all), or stored as spares for future use. The three ranks are described below.

"Good" Chips that pass all the test described in this document are rated "good". Chips rated "good" are to primarily be assembled onto TMCM's.

"Spare" Chips that pass all the test described in this document except for one of the following cases:

- Amplifier gain of one channel is higher than the nominal gain by 25 % or more.
- Amplifier gain of one channel is lower than the nominal gain by 25 % or more.

Chips rated "spare" are to be assembled onto TMCM's if and only if the number of good chips is not sufficient to produce sufficient number of TMCM's.

"Reject" Chips that are not rated either "good" or "spare" are rated "reject". Chips rated "reject" are not to be assembled onto TMCM's.